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(processor same substrate$ same memory
same (less adj area))
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USPT	l1 and (processor with substrate$ with memory with area)	0	L8
USPT	l1 and (processor same integrat$ same substrate$ same memory same area)	24	L7
USPT	l1 and (processor same integrat$ same substrate$ same memory) and coprocessor	1	L6
USPT	l1 and (processor same integrat$ same substrate$ same memory same coprocessor)	0	L5
USPT	l1 and (processor with integrat$ with substrate$ with memory)	5	L4
USPT	l1 and (processor with integrat$ with substrate$)	26	L3
USPT	l1 and (processor same integrat$ same substrate$)	62	L2
USPT	712/$.ccls.	5535	L1

Patent: US004718037

United States Patent [19]

Thaden

[11] **Patent Number: 4,718,037**

[45] **Date of Patent: Jan. 5, 1988**

[54] **MICROCOMPUTER CONTAINING EPROM WITH SELF-PROGRAM CAPABILITY**

[75] Inventor: **Robert C. Thaden, Houston, Tex.**

[73] Assignee: **Texas Instrumens Incorporated, Dallas, Tex.**

[21] Appl. No.: **32,938**

[22] Filed: **Mar. 26, 1987**

Related U.S. Application Data

[63] Continuation of Ser. No. 808,221, Dec. 12, 1985, abandoned, which is a continuation of Ser. No. 365,828, Apr. 5, 1982, abandoned.

[51] **Int. Cl.**[4] **G06F 13/00**

[52] **U.S. Cl.** **364/900**

[58] **Field of Search** ... 364/200 MS File, 900 MS File

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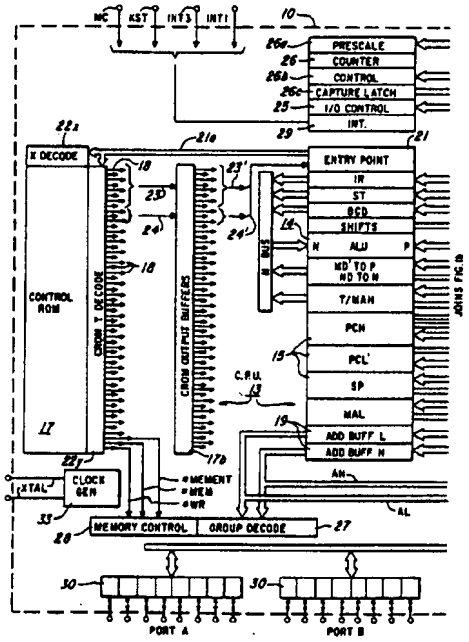
Primary Examiner—Eddie P. Chan

Attorney, Agent, or Firm—Richard K. Robinson; Robert D. Marshall, Jr.; Rodney M. Anderson

[57] **ABSTRACT**

An electronic digital processor system including an internal memory means further including an electrically programmable read-only memory for the storage of data and commands which define operations on the data. Also included is an arithmetic and logic unit for performing operations on the data and a register set for temporary storage of data and addresses. Further included is a plurality of data paths which couple the internal memory with the arithmetic and logic unit and registers. Control and timing circuitry is provided for the execution of commands that access the memory and arithmetic and logic unit by the registers and for the execution of commands for programming the electrically programmable read-only memory.

6 Claims, 22 Drawing Figures



Entry 4 of 5 File: USPT

DOCUMENT-IDENTIFIER: US 4718037 A
TITLE: Microcomputer containing EPROM with self-program capability

BSPR:
In the preferred embodiment, an electronic digital processor system integrated monolithically on a single semiconductor substrate is provided that includes an electrically programmable read-only memory for the storage of data and commands which define operations on the data. The digital processing system also includes an arithmetic and logic unit for performing operations on data which is connected to a register set. The register set is provided for the temporary storage of data and temporary storage of addresses for accessing the memory. The registers, arithmetic and logic unit and memory are interconnected by a plurality of data paths. The digital processor system is controlled by control and timing circuitry which includes the means for executing commands for accessing the memory and arithmetic and logic unit by the register and for executing commands for programming the electrically programmable read-only memory.

CCOR:
712/37

Patent: US005379438

US005379438A

United States Patent [19]

Bell et al.

[11] Patent Number: 5,379,438

[45] Date of Patent: Jan. 3, 1995

[54] **TRANSFERRING A PROCESSING UNIT'S DATA BETWEEN SUBSTRATES IN A PARALLEL PROCESSOR**

[75] Inventors: **Alan G. Bell**, Palo Alto; **John Lamping**, Los Alto, both of Calif.

[73] Assignee: **Xerox Corporation**, Stamford, Conn.

[21] Appl. No.: **629,732**

[22] Filed: **Dec. 14, 1990**

[51] Int. Cl.[6] **G06F 15/16**

[52] U.S. Cl. **395/800**; 395/325; 395/650

[58] Field of Search 395/800, 325, 650

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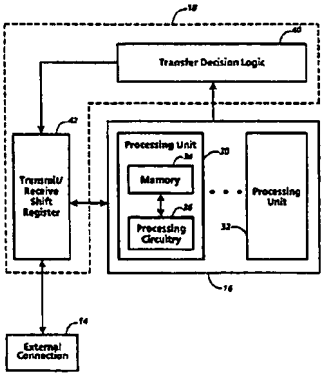
Primary Examiner—Parshotam S. Lall

Assistant Examiner—Viet Vu

[57] **ABSTRACT**

A processor includes interconnected substrates, each with external connecting circuitry and parallel processing circuitry that can perform value assignment search for a set of variables. The parallel processing circuitry includes processing units, each with memory and processing circuitry, and transfer decision logic for determining whether to transfer the data of any of the processing units to another substrate. Each substrate has count logic for counting the processing units whose data indicates a combination of values that could be consistent with constraints being applied, each of which has a valid bit indicating that it could be consistent. The counts are transferred to each connected substrate, and the transfer decision logic at each substrate determines, for each connected substrate, whether to transmit data, receive data, or neither transmit nor receive. The transfer decision logic decides to transfer data only if there are sufficient valid processing units on one substrate and sufficient invalid processing units on the other substrate to ensure that the transfer will succeed. Balancing is performed frequently enough that all substrates have approximately equal numbers of valid processing units. Processing unit selection logic on each substrate selects processing units as sources or destinations, and the select logic can also provide an OR signal. Each pair of connected substrates has a single serial channel, so that one connected substrate transmits its count first, then the other. The same serial channels are used to obtain an intersubstrate count of processing units by assigning each substrate a level in a hierarchy at which it receives sums from some of its connected substrates, operates its own summing logic to add them to its own count, and transmits the resulting sum to another of its connected substrates.

11 Claims, 23 Drawing Sheets



Document Number 1

Entry 1 of 1 File: USPT Jan 3, 1995

DOCUMENT-IDENTIFIER: US 5379438 A
TITLE: Transferring a processing unit's data between substrates in a parallel processor

BSPR:
The present invention provides circuitry on a substrate that can be connected to other components, such as to other similar substrates. The circuitry on the substrate includes parallel processing circuitry with a number of processing units, each able to store and perform operations on respective data. In addition, the circuitry on the substrate includes an external connection and external transfer means For transferring data between any of the processing units and the external connection. The external transfer means can include transfer decision logic for determining whether to transfer the respective data of a processing unit off the substrate. The external connections on a number of substrates can be interconnected to form a coprocessor that can be used in performing value assignment search for a set of variables, with each processing unit's respective data indicating a respective combination of values that could be assigned to the variables.

BSPR:
A processor according to this aspect of the invention can, for example, serve as a coprocessor performing value assignment search in response to a host system. The processor can include a central controller that sends commands to the substrates to control transfers of data and other operations.

DRPR:
FIG. 7 is a schematic block diagram showing components of a system that includes a coprocessor with interconnected substrates.

DEPR:
The general features described in relation to FIGS. 1-6 could be implemented in many ways. Various host systems and interfacing techniques could be used, various substrates could be used, various techniques for forming circuitry at the surface of a substrate could be used, and various types of digital logic could be used. The following description is applicable to any available combination of substrate, processing technology, and logic that is capable of providing an integrated circuit, except where specifically otherwise noted, and is one example of how the general features could be implemented in a processor that could be interfaced in any appropriate way with any host system. The following description builds on features described in copending coassigned U.S. patent application Ser. No. 07/628,916, now issued as U.S. Pat. No. 5,325,500, entitled "Parallel Processing Units on a Substrate, Each Including a Column of Memory" and incorporated herein by reference ("the column processing application").

DEPR:
FIG. 7 shows a system that includes a coprocessor with substrates and a central controller. FIG. 8 shows an example of interconnections between the substrates. FIG. 9 shows host system steps in value assignment search. FIG. 10 shows circuitry in the central controller and in one of the substrates by which the controller and the substrate exchange data.

DEPR:

System 180 in FIG. 7 includes host system 182 and coprocessor 184. Host system 182 could be a Sun or Symbolics workstation or other conventional system capable of executing software requesting value assignment search operations. The Massively Parallel ATMS application, incorporated herein by reference above, explains the operation of a host, including an inference engine that requests propositional reasoning, one type of value assignment search.

DEPR:
Host system 182 can include a VME bus or other conventional interface to which coprocessor 184 can be connected. Coprocessor 184 could include one or more printed circuit boards with appropriate plug connections for connecting to host system 182. Coprocessor 184 includes central controller 186 connected for receiving requests for value assignment search from host system 182 and for providing results of value assignment search to host system 182.

DEPR:
Controller 186 can be a conventional microprocessor or other appropriate component mounted on a printed circuit board and capable of receiving requests for value assignment search from host system 182 and converting the requests into appropriate sequences of commands to substrates 190 through 192. Coprocessor 184 is a single instruction multiple data (SIMD) machine with a large number of simple processing units, with many processing units on each of a large number of substrates. Each processing unit has respective memory that can be thought of as a bit vector, and the controller can determine what each bit position is used for, including the valid bit, described above in relation to FIG. 6. Bit positions can, for example, be used to store data indicating values of basic assumptions, data indicating values of propositions derived from basic assumptions, or temporary data used during value assignment operations.

DEPR:
FIG. 9 shows steps that host system 182 can follow in performing value assignment search using coprocessor 184. The steps in FIG. 9 are independent of the interconnection topology among the substrates.

DEPR:
The step in box 230 receives a call requesting value assignment search using coprocessor 184. This call may come from a routine that applies criteria to determine whether a value assignment search problem can be handled in another way and to determine whether the problem is suitable for solution by coprocessor 184.

DEPR:
The step in box 232 initializes, both by setting up appropriate data structures in host system 182 and also by providing a request to coprocessor 184 for initialization. The step in box 232 can include operations that parse the constraints to be applied during value assignment search into parts, each of which can be treated as a constraint in the remaining steps in FIG. 9. For example, if each original constraint is converted to a conjunctive normal form in which it is a conjunction of disjunctions of simple variables, the step in box 232 can parse the original constraint so that each disjunction is treated as a constraint.

DEPR:
The choice of which variable to fork can be based on the number of processing units that could fork on the variable and on the number of processed constraints that include the variable. Host system 182 can obtain information about the number of forking processing units by providing requests to coprocessor 184 that cause it to provide pertinent data. In general, the variable that has the least forking processing units and the most affected processed constraints is the best choice. A variable with no affected processed constraints should not be forked because forking it will increase the number of valid processing units without leading to any further killing of inconsistent processing units. An implementation of forking is described below.

DEPR:
The step in box 250 then applies one of the pending constraints, kills any processing units that are inconsistent, and makes the applied constraint a processed constraint. In this step, host system 182 provides requests to coprocessor 184 to perform logical or arithmetic operations that apply the

constraint and obtain data indicating whether each processing unit is inconsistent with the constraint, and then to perform an operation that kills inconsistent processing units. To apply the constraint and to kill, host system 182 can request that controller 186 provide commands of the form:

DEPR:
When all of the constraints are satisfied, the step in box 270 provides requests to coprocessor 184 to obtain results based on the data in the processing units' memories. An implementation of obtaining results is described below. Then host system 182 determines in box 272 whether pruning was performed in box 246. If so, a new search is begun with the step in box 232, except that the variable that was forced to one value by pruning is forced to its other value for the new search, which can be done with calculate commands. If pruning was performed more than once, each possible combination of the variables forced during pruning must be handled by a new search: If two variables were forced, three additional combinations must be handled; if three were forced, seven additional combinations must be handled; and so forth.

DEPR:
Many of the steps in FIG. 11 can be performed by host system 182, since it can manage the variables and constraints without reference to coprocessor 184. But some of the steps require operations by central controller 186 and processing units on substrates 190 through 192. Specifically, the steps in boxes 374, 380, and 390 all require information about processing units with data meeting a criterion, which can be obtained by hierarchical operations as discussed immediately below. An implementation of the balancing step in box 384 is also described below and an implementation of forking in box 392 is described in the column processing application incorporated herein by reference.

DEPR:
Configuration of the substrates could be performed in a number of ways. To minimize configuration time when coprocessor 184 is being used, all necessary data for startup could be stored in ROM on each substrate. But this would seriously limit the flexibility of interconnection between substrates, and would cause problems in case one substrate malfunctions. Therefore, the implementation described below stores relatively little data on each substrate prior to initialization, but makes use of circuitry described above to obtain configuration data.

DEPC:
1. Coprocessor

CCOR:
712/16

CCXR:
712/13

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Document Number 1

Entry 1 of 5 File: USPT Dec 23, 1997

DOCUMENT-IDENTIFIER: US 5701425 A
TITLE: Data processor with functional register and data processing method

DEPR:
FIG. 9 is a block diagram showing one embodiment of the data processor using the functional registers which have been described with reference to FIGS. 2 to 8. The data processor, is formed on a single semiconductor substrate by the well-known semiconductor integrated circuit manufacturing technology and is illustrated to include: an instruction control part 1; an operation part 2; an instruction cache memory 3; and a data cache memory 4.

CCOR:
712/200

CCXR:
712/245

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Entry 2 of 5 File: USPT Dec 6, 1994

DOCUMENT-IDENTIFIER: US 5371894 A
TITLE: Off-chip breakpoint system for a pipelined microprocessor

CLPR:
1. In a pipelined processor system of a type including an integrated circuit pipelined microprocessor located on a first substrate and an instruction cache and memory management unit (CMMU) located on a second substrate, different from said first substrate, where code addresses are sent to the instruction CMMU and the instruction CMMU returns with code instructions and returns with a FAULT code reply signal when there is no reply code, and wherein an exception is forced to the pipelined microprocessor in response to the FAULT code reply signal, a breakpoint system for providing a breakpoint exception at a predetermined instruction address, said breakpoint system comprising:

CLPR:
9. A method for providing a hardware assisted breakpoint facility in a processor system of a type including an integrated circuit pipelined microprocessor, located on a first substrate, and an instruction cache and memory management unit (CMMU) located on a second substrate, different from said first substrate, wherein code addresses are sent to the instruction CMMU and the instruction CMMU returns with code instructions and with a code reply signal, and wherein the pipelined microprocessor is forced to take an exception by a FAULT code reply signal, said method comprising the steps of:

CCXR:
712/42

Entry 5 of 5 File: USPT

DOCUMENT-IDENTIFIER: US 4680698 A
TITLE: High density ROM in separate isolation well on single with chip

CLPR:
2. A microcomputer comprising an on-chip processor and on-chip memory on a single integrated circuit chip having a substrate of semiconductor material of a first type, wherein said on-chip memory comprises a high density RAM array having at least 1K bytes for holding a program containing instructions for execution by said on-chip processor, said microcomputer including:

CCOR:
712/37

Entry 3 of 5 File: USPT Jul 6, 1993

DOCUMENT-IDENTIFIER: US 5226173 A
TITLE: Integrated data processor having mode control register for controlling operation mode of serial communication unit

CLPR:
4. In an integrated protocol processor including, on a single semiconductor substrate, an input terminal for receiving input serial data from outside the integrated protocol processor, an output terminal for supplying output serial data to the outside of the integrated protocol processor, a bus, a central processing unit coupled to the bus, a direct memory access controller coupled to the bus, a timer circuit coupled to the bus, and a serial communication unit coupled to the bus and to the input and output terminals for receiving the input serial data from the input terminal and for sending the output serial data to the output terminal, the integrated protocol processor comprising:

CCOR:
712/40